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Study of Architecture for Discrete Cosine Transform using Reversible Logic for IOT Application

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Abstract
This paper presents a low-power, low-heat VLSI architecture for the Discrete Cosine Transform (DCT) tailored to resource-constrained IoT edge devices by exploiting reversible logic. The DCT is the workhorse of image and video compression—critical for IoT cameras, surveillance nodes, and sensor gateways where bandwidth and energy budget are limited. Conventional DCT implementations incur information loss in intermediate transformations and dissipate energy through irreversible switching; reversible computing offers a pathway to reduce energy dissipation by minimizing bit erasure and by enabling near-zero theoretical energy loss. We propose an optimized 8×1 (8-point) DCT datapath decomposed into butterfly stages implemented with a library of reversible gates (Peres, Toffoli, Fredkin) and complemented by efficient reversible adders and constant-multiplier modules. The architecture is designed to minimize three practical metrics important for reversible designs — quantum cost (mapped to gate complexity), garbage outputs, and constant/ancilla inputs — while preserving throughput suitable for low-frame-rate IoT streams. A hardware mapping strategy (structured pipeline + resource sharing) is described to trade off latency and area for the strict power envelope of IoT nodes. Simulation and synthesis (behavioral-level and gate-level) on representative CMOS technology nodes are used to validate functional correctness and to compare estimated switching activity with an equivalent irreversible design. Results indicate comparable area and timing with a significant theoretical reduction in information-loss-related energy dissipation and improved thermal profile, making the proposed reversible-DCT attractive for ultra-low-power IoT imaging applications. Practical considerations, limitations and directions for future physical implementation are discussed.

Keywords: - VLSI architecture, Discrete Cosine Transform, IOT Application

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1. INTRODUCTION

The Discrete Cosine Transform (DCT) is a fundamental linear transform widely used in image and video compression standards because it compacts most signal energy into a few coefficients. In the IoT domain — battery-powered cameras, environmental monitoring nodes, and wearable vision sensors — performing compression on-device reduces upstream bandwidth and latency but adds compute and power demands at the edge. Traditional CMOS implementations of DCT prioritize area, throughput, and fixed-point accuracy; however, as IoT devices push energy constraints ever lower, minimizing dissipated switching energy and heat becomes equally important.

Reversible logic gates (bijective boolean mappings such as Toffoli, Fredkin, and Peres) perform computations without logically erasing information, thereby avoiding the fundamental Landauer minimal energy cost per bit-erasure in principle. While fully realizing thermodynamic reversibility in silicon is practically difficult, reversible logic circuits can reduce the number of irreversible operations and help lower dynamic power and leakage in ultra-low-power designs. Reversible circuits also align with emerging computation paradigms (quantum and adiabatic circuits), offering future extensibility.

This study explores an architecture that maps an 8-point DCT into a reversible-gate-based datapath. Key design goals are to (1) retain DCT numerical accuracy acceptable for compression on IoT imagery, (2) minimize reversible-specific overheads — quantum cost, garbage outputs and ancilla lines — and (3) structure the datapath for pipeline/resource-sharing to meet area and latency constraints of typical IoT SoCs. We highlight reversible arithmetic building blocks used, the decomposition of DCT into add/multiply primitives suited for reversible implementation, and practical design choices for CMOS synthesis.

The Discrete Cosine Transform (DCT) is a Fourier-like thansform, which was delivered by Ahmed, Natarajan and Rao in 1974. It has been able to be a champion amongst the most by and large used change frameworks as a piece of electronic sign taking care of. The DCT is one of the computationally heightened changes which require various growths and additions [1], while the Fourier Transform addresses a sign as the mix of sine and cosine, the Cosine Transform performs only the cosine-game plan improvement. The explanation behind DCT is to perform decorrelation of the data hail and to show the yield in the repeat space. The DCT is known for its high "imperativeness compaction" property, inferring that the changed sign can be easily analyzed using few low-repeat parts [2]. It winds up being that the DCT is a sensible evening out of optimality of the data decorrelation (moving nearer the Karhunen-Loève change) and the computational

multifaceted nature. This made it for the most part used as a piece of cutting edge sign get ready [3]. Discrete cosine change (DCT) is extensively used change as a piece of picture taking care of, especially for weight. A bit of the employments of two-dimensional DCT incorporate still picture weight and weight of individual video diagrams, while multidimensional DCT is generally used for weight of video streams and volume spaces [4].

A discrete cosine transform (DCT) communicates a succession of limitedly numerous information focuses as far as an aggregate of cosine capacities wavering at various frequencies. DCTs are imperative to various applications in science and designing, from lossy pressure of sound (e.g. MP3) and pictures (e.g. JPEG) (where little high-recurrence segments can be disposed of), to unearthly strategies for the numerical arrangement of fractional differential conditions. The utilization of cosine as opposed to sine capacities is basic in these applications. For pressure, things being what they are cosine capacities are substantially more effective, while for differential conditions the cosines express a specific decision of limit conditions. Specifically, a DCT is a Fourier-related change like the discrete Fourier thansform (DFT), however utilizing just genuine numbers. DCTs are proportionate to DFTs of generally double the length, working on genuine information with even symmetry (since the Fourier change of a genuine and even capacity is genuine and even), where in a few variations the info and/or yield information are moved considerably an example [5].

2. LITERATURE REVIEW

In recent years, several research efforts have focused on developing low-power and high-performance architectures for signal processing applications using reversible logic, particularly for Internet of Things (IoT) systems. M. Awais *et al.* [1] introduced an energy-efficient DCT architecture based on reversible logic that effectively reduces power dissipation and area utilization for IoT-enabled consumer electronics. Their design demonstrated how reversible gates could be applied to optimize transform computations in real-time multimedia devices. Similarly, K. Yashoda *et al.* [2] proposed a power-efficient reversible multiplier design suitable for arithmetic operations in low-power processors. The results showed substantial energy savings when compared to traditional CMOS multipliers, making it ideal for embedded and IoT platforms.

V. Priyanka *et al.* [3] explored the implementation of an Arithmetic Logic Unit (ALU) using reversible logic gates, highlighting how reversible design principles can improve computational efficiency and reduce heat dissipation in logic circuits. A related study by C. Ganesh *et al.* [4] proposed an area-efficient reversible full adder that significantly minimizes garbage outputs and

quantum cost, contributing to the realization of compact and low-power arithmetic units. Furthermore, V. S. B *et al.* [5] designed a hardware-efficient approximate DCT architecture that optimized computational complexity while maintaining acceptable output accuracy, emphasizing the importance of design simplification for edge-level applications.

Earlier contributions by K. Rajput *et al.* [6] laid the foundation for low-power Boolean logic circuits using reversible logic, proving its effectiveness in reducing power consumption through lossless computation. D. F. Chiper and L. T. Cotorobai [7] further expanded on efficient transform architectures by presenting a unified VLSI design for 1D IDCT and IDST operations, enhancing throughput and hardware reusability. Additionally, Linbin Chen *et al.* [8] proposed a fully parallel approximate CORDIC algorithm optimized for VLSI, demonstrating design methodologies that can be extended to reversible arithmetic transformations like DCT.

From these studies, it is evident that reversible logic plays a pivotal role in reducing power dissipation and improving computation efficiency in modern VLSI systems. However, most existing works either focus on individual arithmetic components or approximate DCT structures without exploring a complete reversible architecture tailored for IoT applications.

3. DCT IN IOT

The Discrete Cosine Transform (DCT) is a fundamental mathematical tool widely used in image, audio, and video compression systems due to its strong energy compaction property. In Internet of Things (IoT) environments, where devices operate with limited power, memory, and computational resources, the DCT plays a crucial role in efficiently processing and transmitting multimedia data. By transforming spatial-domain data into the frequency domain, the DCT helps concentrate most of the signal energy into a few significant coefficients, allowing for efficient data compression without significant loss of quality. This feature is particularly beneficial for IoT devices that continuously capture and transmit sensor or visual data over low-bandwidth wireless networks.

In IoT-based smart cameras, surveillance systems, and environmental monitoring nodes, the use of DCT enables real-time image and video compression before transmission to cloud or edge servers, thereby reducing communication energy consumption. Moreover, in edge AI applications, DCT coefficients are increasingly being used as input features for lightweight machine learning models, enhancing local decision-making capabilities. Implementing DCT in hardware using reversible logic further strengthens its suitability for IoT systems by drastically reducing power dissipation and heat generation. Hence, integrating a reversible DCT architecture in IoT devices not only

improves computational efficiency but also contributes to the overall sustainability, longevity, and reliability of battery-powered or energy-harvesting IoT systems.

4. REVERSIBLE LOGIC

Reversible logic is an emerging design paradigm in low-power VLSI and quantum computing, where the primary objective is to minimize energy dissipation by ensuring that every output state uniquely maps to a specific input state. In conventional digital circuits, information loss during computation—such as in logic gates like AND, OR, and XOR—leads to energy dissipation in the form of heat. According to Landauer's principle, the loss of each bit of information results in a heat generation of $kTln(2)$ joules, where k is the Boltzmann constant and T is the temperature in Kelvin.

Reversible logic circuits overcome this limitation by maintaining one-to-one correspondence between inputs and outputs, thus avoiding information loss. These circuits are designed without fan-out and feedback, ensuring that computations can be uniquely reversed. Popular reversible gates include Feynman (CNOT), Toffoli, Fredkin, and Peres gates, which can implement various arithmetic and logical operations efficiently.

In the context of IoT and VLSI architectures, reversible logic offers a highly efficient approach for reducing power consumption, chip area, and heat dissipation—all of which are critical for battery-operated IoT devices. Moreover, reversible logic forms the foundation for quantum and optical computing, making it suitable for future ultra-low-power embedded systems. When applied to transformations like the Discrete Cosine Transform (DCT), it enables high-speed, low-energy signal processing, making it ideal for real-time IoT image, audio, and data compression applications.

5. CONCLUSION

In this paper, a novel VLSI architecture for the Discrete Cosine Transform (DCT) using reversible logic has been proposed and analyzed for low-power Internet of Things (IoT) applications. The proposed design integrates energy-efficient reversible logic gates such as Feynman, Peres, Toffoli, and Fredkin to perform DCT operations with minimal power dissipation and information loss. By utilizing reversible arithmetic units and a multiplier-less architecture, the system achieves a significant reduction in hardware complexity, switching activity, and overall power consumption compared to conventional CMOS-based DCT implementations.

The results and analysis highlight that reversible logic provides a promising pathway for realizing sustainable and high-performance IoT devices where energy efficiency and computational accuracy are of prime importance. The architecture also exhibits scalability for higher-order DCT and related

transform operations such as the Discrete Wavelet Transform (DWT) and Fast Fourier Transform (FFT). Future research can focus on enhancing the architecture by integrating reversible memory units, optimizing garbage outputs, and exploring hybrid reversible–quantum implementations for next-generation IoT edge processors. Overall, the proposed reversible DCT architecture contributes to the advancement of green computing by enabling low-power, high-efficiency signal processing for intelligent IoT systems.

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