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VHDL Implementation of Reversible Arithmetic Logic Unit using Bidirectional Gate

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Abstract- Reversible computing is a promising approach to addressing the challenges of energy dissipation and efficiency in modern digital systems. This study explores the design and VHDL implementation of a Reversible Arithmetic Logic Unit (RALU) using bidirectional gates. The proposed RALU architecture integrates arithmetic and logical operations with reversibility, ensuring minimal power loss and enhanced computational efficiency. By leveraging the unique properties of bidirectional gates, the design achieves reduced quantum cost, gate count, and propagation delay compared to traditional ALU designs. The VHDL implementation provides a hardware description that can be synthesized and tested on FPGA platforms, offering insights into its practical applicability in low-power and quantum computing environments. Simulation results validate the correctness and performance of the proposed RALU, demonstrating its potential for use in advanced computing systems, including cryptography, quantum processors, and energy-efficient embedded systems. In this paper, the two novel 4*4 reversible logic gates (HNG and PFAG) are used with minimal delay, and may be configured to produce a variety of logical calculations on fixed output lines based on programmable select input lines. The proposed RALU design is verified and its advantages over the only existing ALU design are quantitatively analyzed. The proposed design is synthesized using Xilinx ISE software.

Keywords—Reversible Gates, Arithmetic Unit (ALU), Number of Slice, Look Up Table

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INTRODUCTION

Reversible computing has emerged as a critical area of research due to its potential to address the challenges of energy dissipation in digital systems. Traditional computing architectures inherently lose energy during computation due to the erasure of bits, as per Landauer's principle. In contrast, reversible computing ensures that no information is lost, thereby minimizing energy loss and heat generation [1, 2]. This principle makes reversible logic an essential component for developing energy-efficient systems, particularly in quantum computing, cryptographic systems, and low-power VLSI designs. This study focuses on the design and implementation of a Reversible Arithmetic Logic Unit (RALU) using bidirectional gates. Bidirectional gates offer unique advantages in reversible computing by enabling efficient data flow and operation reversibility, thereby reducing gate count and quantum cost [3, 4]. The RALU integrates arithmetic and logical functions, providing a versatile and efficient solution for modern computational challenges. By utilizing VHDL for the hardware description, this work aims to provide a practical implementation of the proposed design, validating its performance through simulation and synthesis. The findings of this research contribute to advancing reversible computing and its applications in next-generation energy-efficient systems.

REVERSIBLE GATES

Reversible logic is one such possible computing technique in order to overcome the above discussed challenges. In reversible logic, it requires an equal number of inputs and outputs. Reversible computation has the provision to reproduce the input from the output. Conventionally available, the simplest example of reversible computation is ‘NOT’ gate.

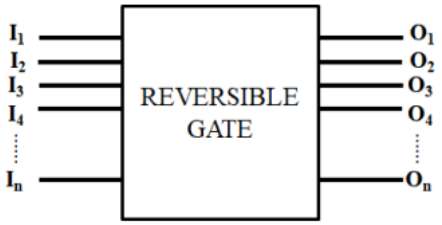

Figure 1: Generic structure of Reversible Gate

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It produces logic '0' for the input '1'; by applying this output '0' to the input, it is possible to reproduce the input. So 'NOT' gate is a conventionally available Reversible Gate. So, when the number of inputs and outputs are equal, then there is no heat dissipation according to Landauer's principle (Landauer 1961). A reversible gate consists of an equal number of inputs and number of outputs [3, 4]. The size of the reversible gate is defined by the number inputs/outputs. The general structure of reversible gate is shown in Figure 1, where I_1, $I_{2...}$ I_n are inputs and O_1, O_2…. O_n are outputs of the reversible gate. For particular i, there exists a relation Ii → O_i [5].

The realization of the reversible logic circuits needs to be low power, high speed and beyond Landauer energy limit. One such nanotechnology is Quantum Cellular Automata (QCA); where information is stored in the form of polarity in the small quantum dots. The information processing and propagation in QCA are by means of electrostatic force (Coulomb interaction) between the adjacent dots [6]. Hence, in this Thesis, we are focusing on the Reversible logic-based circuit design and its realization in QCA.

○ BASIC REVERSIBLE GATES

Several reversible gates have come out in the recent years. The most basic reversible gate is the Feynman gate and is shown in Fig. 2. It is the only 2x2 reversible gate available and is commonly used for fan out purposes. Consider the input B as constant. When B is zero, the gate acts as a copying gate or a buffer where both the output lines contain the input A. When B is one, the complement of A is obtained at the output Q. The 3x3 reversible gates include Toffoli gate, Fredkin gate, New gate and Peres gate, all of which can be used to realize various Boolean functions. Fredkin gate is shown in Fig. 3. The 4x4 reversible gates include TSG gate, MKG gate, HNG gate, PFAG gate etc.

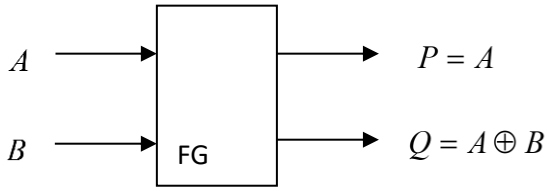

Figure 2: Feynman gate

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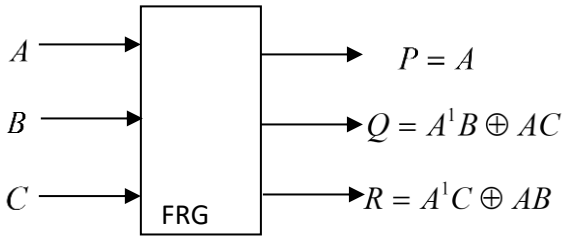

Figure 3: Fredkin gate

Figure 4 shows the Peres gate. Some of the 3x3 gates are designed for implementing some important combinational functions in addition to the basic functions. Most of the above-mentioned gates can be used in the design of reversible adders.

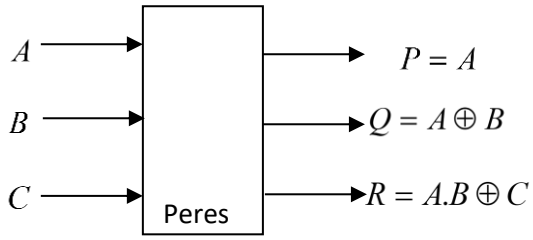

Figure 4: Peres gate

Several 4x4 gates have been described in the literature targeting low cost and delay which may be implemented in a programmable manner to produce a high number of logical calculations. The HNG gate, presented in [10], produces the following logical output calculations:

$$P = A \quad (1)$$

$$Q = B \quad (2)$$

$$R = A \oplus B \oplus C \quad (3)$$

$$S = (A \oplus B).C \oplus (AB \oplus D) \quad (4)$$

The quantum cost and delay of the HNG is 6. When $D = 0$, the logical calculations produced on the R and S outputs are the required sum and carry-out operations for a full adder. The block diagram representation of the HNG is presented in Fig. 5.

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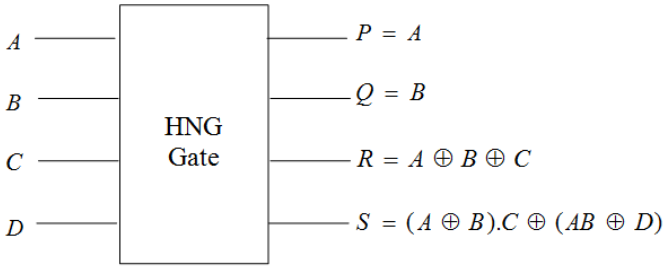

Figure 5: HNG Gate

A new programmable 4x4 reversible logic structure - Peres And-Or (PFAG) gate – is presented which produces outputs

$$P = A \quad (5)$$

$$Q = A \oplus B \quad (6)$$

$$R = A \oplus B \oplus C \quad (7)$$

$$S = (A \oplus B)C \oplus AB \oplus D \quad (8)$$

Figure 6 shows the block diagram of the PFAG gate. This gate is an extension of the Peres gate for ALU realization.

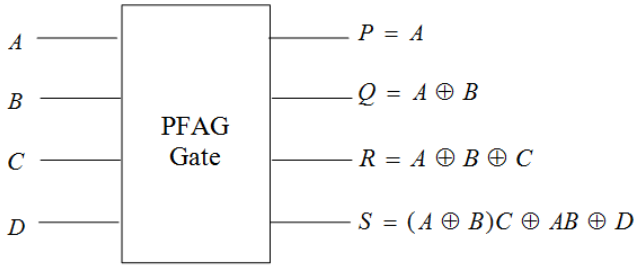

Figure 6: PFAG Gate

REVERSIBLE ALU DESIGN

ALU works as a data processing components which is an important part in the central process unit (CPU). Besides, it is the main performer in any computing devices. ALU is a multi-functional circuit that performs one of a few possible functions on two operands of A and B which is depending on the control inputs.

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The S2, S1 and S0 are the selection lines while Cin is the input carry. Input A and B are the data input for the ALU design. Based on the truth table shown in Table 1, when selection line S2 is equal to zero, the circuit performs eight arithmetic operations and when selection line S2 is equal to one, the circuit performs the logic operations of OR, EX-OR, AND and NOT functions.

Table 1: Function table of ALU

S2	S1	S0	Cin	Operation	Function
0	0	0	0	F=A	Transfer A
0	0	0	1	F=A+1	Increment A
0	0	1	0	F=A+B	Addition
0	0	1	1	F=A+B+1	Add with carry
0	1	0	0	F=A+B’	Subtract with borrow
0	1	0	1	F=A+B’+1	Subtraction
0	1	1	0	F=A-1	Decrement A
0	1	1	1	F=A	NAND
1	0	0	0	F=A^B	OR
1	0	0	1	F=AʘB	EX-OR
1	0	1	0	F=A&B	AND
1	0	1	1	F=A’	NOT

The proposed reversible ALU is designed to produce the same function as implemented by conventional ALU. Figure 7 is the block diagram of proposed reversible ALU designs. It has two main logic circuit design, namely, control unit and reversible full adder and the proposed design has five constants signals (e.g: Cinput1, Cinput2, Cinput3, Cinput4 and Cinput5) with a provision for realizing the eight arithmetic operations and four logic operations.

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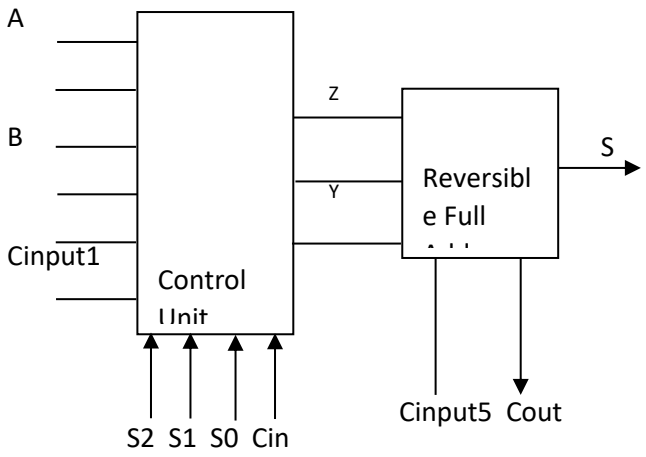

Figure 7: Block Diagram of RALU Design

(i) Control Unit

Control unit is a critical part in the reversible ALU design. Control unit performs the arithmetic operations inside the ALU. As shown in Fig.8, the proposed control unit design is made up from three Feynman gates, three R-I gates and one Fredkin gate. Four control variables S2, S1, S0 and Cin select twelve different operations in the reversible ALU design. The arithmetic and logic operations are differentiated using the variable input of S2. The control unit has four constant signals. There are eight garbage outputs in the proposed control unit logic circuit.

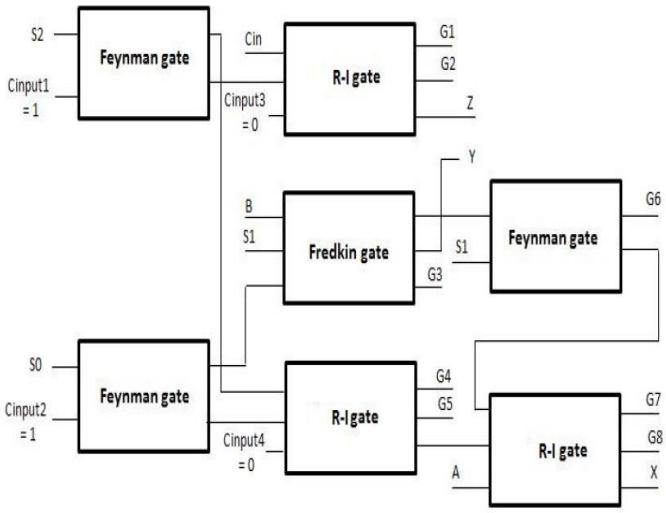

Figure 8: Block diagram of control unit

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SIMULATION RESULTS

In the figure 9 and figure 10 show the view technology schematic and resistor transfer level of 1-bit ralu based on hng, input of the reversible arithmetic logic unit (ralu) is represented by a1, b1, previous carry of the ralu is represented by cin1, select line of the ralu is represented by s11, s12 and s13 and output of the ralu is represented by result respectively.

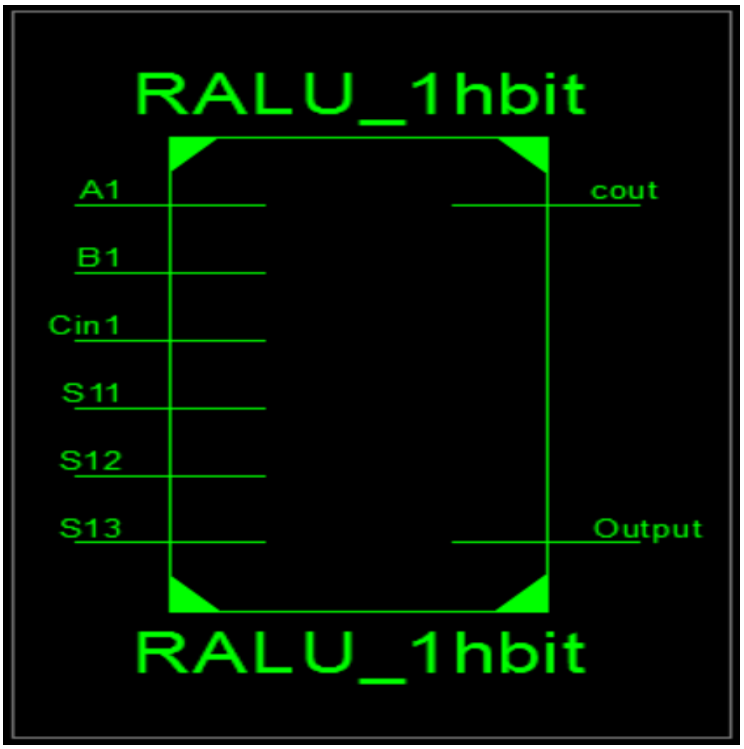

Figure 9: View Technology Schematic for 1-bit RALU

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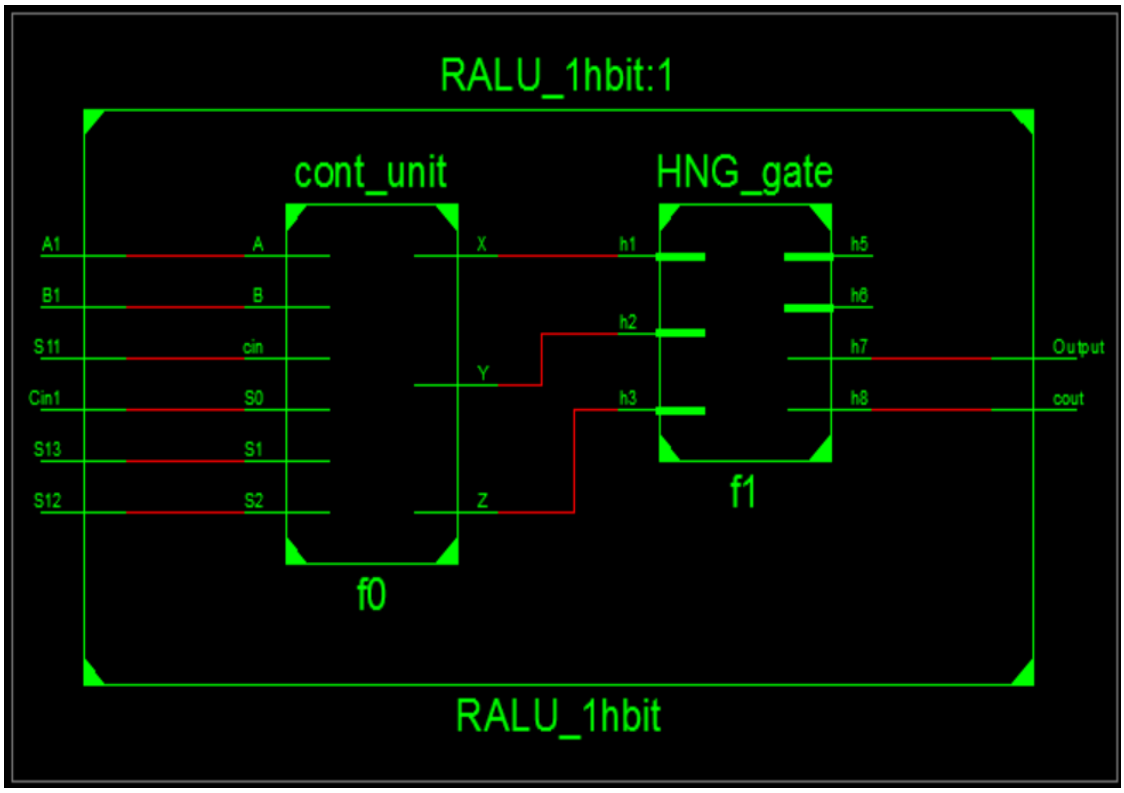

Figure 10: RTL View for 1-bit RALU

Table 2: Proposed Design based on HNG Gate

Number of Bits	Reversible ALU Design for HNG Gate	Reversible ALU Design for PFAG Gate	Conventional ALU (ns)
1-bit	1.044	1.044 ns	7.17 ns
4-bit	3.478	3.580 ns	8.13 ns
8-bit	5.790	5.892 ns	8.29 ns
16-bit	10.440	10.542 ns	12.34 ns
32-bit	19.695	19.995	24.995
64-bit	38.205	38.705	42.705
128-bit	75.224	75.824	81.824

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256-bit	140.260	140.860	145.860
512-bit	297.261	297.961	302.961

CONCLUSION

This research successfully demonstrated the design and VHDL implementation of a Reversible Arithmetic Logic Unit (RALU) utilizing bidirectional gates, paving the way for advancements in energy-efficient and sustainable computing. The proposed RALU architecture efficiently integrates arithmetic and logical operations with reversible logic, achieving reduced quantum cost, gate count, and delay. The use of bidirectional gates enhances the design's versatility and scalability, making it a suitable candidate for next-generation computing systems. The VHDL implementation and simulation results validate the functional correctness and performance of the proposed RALU. This work highlights its applicability in quantum computing, low-power embedded systems, and cryptographic applications, where energy efficiency and minimal heat dissipation are critical. Future work could focus on further optimizing the gate-level architecture, extending the RALU's functionality, and exploring its deployment in real-world hardware platforms such as FPGAs and ASICs. The simulation results illustrate that the proposed reversible ALU design 2 outperforms the proposed reversible ALU design 1 and conventional ALU design.

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