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Review on Reversible Radix-2 FFT using Reversible Gate and Different Adder

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Abstract— Reversible computing has emerged as a promising approach for designing low-power and energy-efficient digital circuits by minimizing information loss and reducing heat dissipation. In Very Large-Scale Integration (VLSI) systems, Reversible Logic Gates have gained considerable attention due to their potential applications in quantum computing, nanotechnology, digital signal processing (DSP), and low-power hardware architectures. Among DSP algorithms, the Radix-2 Fast Fourier Transform (FFT) is one of the most widely used techniques for efficient computation of the Discrete Fourier Transform (DFT), playing a vital role in wireless communication, image processing, biomedical engineering, radar, and multimedia applications. The performance of a reversible Radix-2 FFT architecture is largely influenced by the efficiency of the reversible butterfly unit and the reversible adder employed during arithmetic operations.

This review presents a comprehensive analysis of Reversible Radix-2 FFT architectures implemented using various reversible logic gates, including Feynman Gate (FG), Fredkin Gate (FRG), Toffoli Gate (TG), Peres Gate (PG), HNG Gate, TSG Gate, and BKG Gate, along with different reversible adder designs such as Ripple Carry Adder (RCA), Carry Look-Ahead Adder (CLA), Carry Save Adder (CSA), Carry Select Adder (CSLA), and Modified Carry Select Adder (MCSLA). The review compares existing architectures based on important design metrics, including quantum cost, garbage outputs, constant inputs, propagation delay, power consumption, silicon area, and hardware complexity. Furthermore, recent optimization techniques aimed at reducing quantum cost and improving computational efficiency are critically discussed.

Keywords— FFT, Decimation in Time, Decimation in Frequency, Reversible Gate

I. INTRODUCTION

The Fast Fourier Transform (FFT) is one of the most widely used algorithms in digital signal processing (DSP) for efficiently computing the Discrete Fourier Transform (DFT) and its inverse. FFT plays a crucial role in numerous applications, including wireless communication, orthogonal frequency division multiplexing (OFDM), radar systems, image and video processing, biomedical signal analysis, audio processing, and real-time embedded systems. Compared with the direct computation of DFT, which requires arithmetic

operations, the FFT reduces the computational complexity to, making it highly suitable for high-speed signal processing. Among the various FFT algorithms, the Radix-2 FFT is the most implemented architecture due to its simple butterfly structure, modularity, and ease of hardware realization [1, 2].

With the continuous advancement of Very Large-Scale Integration (VLSI) technology, the demand for high-performance and energy-efficient digital circuits has increased significantly. However, conventional CMOS-based logic circuits suffer from unavoidable energy dissipation caused by information loss during computation. According to Landauer's principle, every bit of information erased in an irreversible logic circuit results in a minimum energy loss of, where is Boltzmann's constant and is the absolute temperature. To overcome this limitation, reversible logic has emerged as a promising design paradigm that enables one-to-one input-output mapping, thereby avoiding information loss and significantly reducing power dissipation. Reversible logic has become a key technology for quantum computing, nanotechnology, optical computing, low-power VLSI systems, and next-generation signal processing architectures [3, 4].

Several reversible logic gates have been developed to implement arithmetic and logical operations efficiently. Commonly used reversible gates include the Feynman Gate (FG), Toffoli Gate (TG), Fredkin Gate (FRG), Peres Gate (PG), HNG Gate, TSG Gate, and BKG Gate. These gates are widely employed in the design of reversible adders, multipliers, multiplexers, and butterfly processing units. Since addition is one of the most frequently performed operations in FFT computation, the choice of reversible adder has a significant impact on the overall performance of the FFT processor. Researchers have proposed various reversible adder architectures, including Ripple Carry Adders (RCA), Carry Look-Ahead Adders (CLA), Carry Save Adders (CSA), Carry Select Adders (CSLA), and Modified Carry Select Adders (MCSLA), to improve computational speed while reducing quantum cost, garbage outputs, constant inputs, and hardware complexity [5, 6].

In recent years, considerable research has focused on integrating reversible logic into Radix-2 FFT architectures to achieve high-speed and low-power signal processing. Existing studies have investigated different combinations of reversible butterfly structures and reversible arithmetic units to optimize design parameters such as quantum cost, propagation delay, power consumption, gate count, garbage outputs, constant inputs, and silicon area. Despite these developments, there remains a need for a comprehensive review that systematically compares reversible Radix-2 FFT architectures using different reversible gates and reversible adder designs while identifying current challenges and future research opportunities [7].

This review provides a comprehensive survey of Reversible Radix-2 FFT architectures implemented using various reversible logic gates and different reversible adder structures. The paper critically analyzes published research based on performance metrics including quantum cost, garbage outputs, constant inputs, propagation delay, power consumption, area utilization, and hardware complexity. Furthermore, the advantages, limitations, and design trade-offs of existing approaches are discussed, and potential research directions are highlighted for developing scalable, high-speed, and energy-efficient reversible FFT

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processors. The findings of this review are expected to assist researchers in designing optimized reversible FFT architectures for applications in quantum computing, nanotechnology, digital signal processing, artificial intelligence, and future low-power VLSI systems [8, 9].

II. FFT ALGORITHM

A FFT is a calculation to process the discrete Fourier change (DFT) and its reverse. Fourier investigation changes over time (or space) to recurrence and the other way around; a FFT quickly registers such changes by factorizing the DFT framework into a result of scanty (for the most part zero) factors. Subsequently, quick Fourier changes are broadly utilized for some applications in building, science, and arithmetic. Demonstrate the butterfly tasks for radix-2 DIF FFT in figure 1 and figure 2. The radix-2 calculations are the most straightforward FFT butterfly calculation.

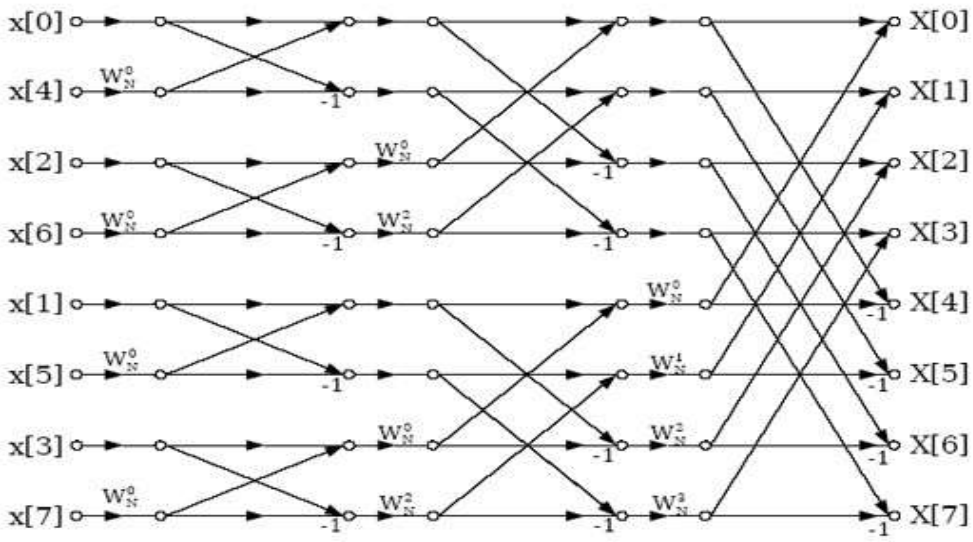

Figure 1: Radix-2 Decimation in Time Domain FFT

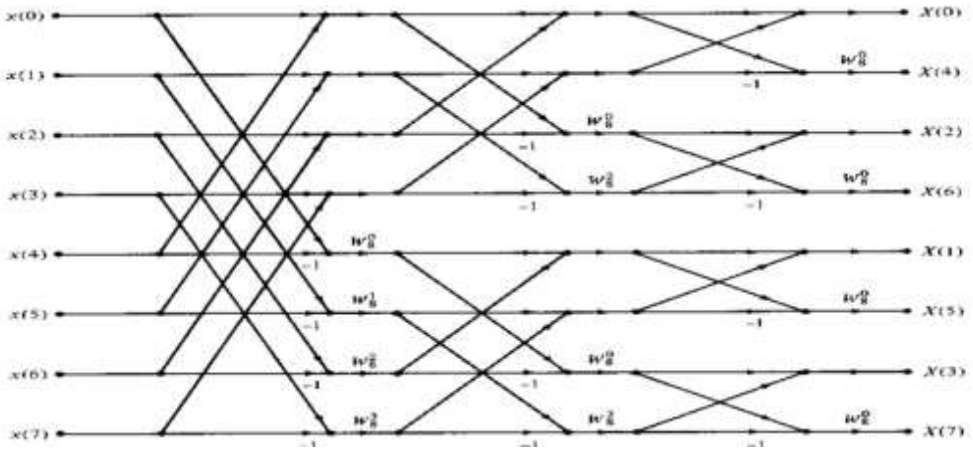

Figure 2: Radix-2 Decimation in Frequency Domain FFT

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Radix-2

Troublesome to recognize from one another, for this situation the zone based methodology will be calm valuable. Standardized cross connection [13] is a broadly utilized methodology in the territory based technique. Consolidating the stage relationship strategy with methodology was pro acted like an advancement territory based technique interpretation, scale and revolution. Utilized a likelihood thickness inclination based interest direct indicator toward remove the steady point highlights.

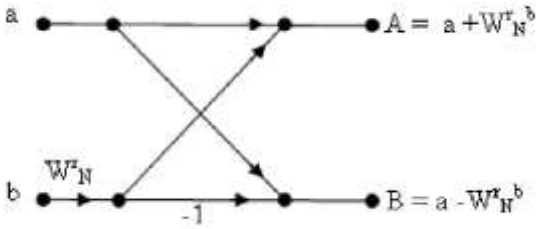

Figure 3: Computation of Butterfly using Radix-2

They proposed worldwide parallax histogram based channel to dispose of the anomaly actuated by old style connection strategy. They strategy that utilizations bootstrap resampling to gauge the vulnerability of territory put together picture enlistment calculation with respect to a specific pair of pictures. He proposed a strategy for programmed enlistment. In this, they first applied Harris administrator to remove the corner highlights after that canny administrator is executed to identify the picture edges. The relationship be tween's the picture sets yields the corner focuses. The relative change between the picture pair is set up, which figures the boundaries, as per that the pictures are enlisted.

III. METHODOLOGY

This review follows a systematic methodology to analyze and compare existing Reversible Radix-2 FFT architectures implemented using various reversible logic gates and reversible adder designs. Initially, relevant research articles published in IEEE, Springer, Elsevier, ACM, and other reputed journals and conferences were collected. The selected studies primarily focus on the implementation of Radix-2 FFT using reversible logic for low-power and high-speed VLSI applications. The collected literature was screened based on publication quality, novelty, and the availability of hardware performance metrics.

After selecting the relevant publications, the architectures were classified according to the type of reversible logic gates, including Feynman Gate (FG), Toffoli Gate (TG), Fredkin Gate (FRG), Peres Gate (PG), HNG Gate, TSG Gate, and BKG Gate. Similarly, the arithmetic units used in the butterfly processor were categorized based on different reversible adder architectures, such as Ripple Carry Adder (RCA), Carry Look-Ahead Adder (CLA), Carry Save Adder (CSA), Carry Select Adder (CSLA), and Modified Carry Select Adder (MCSLA). Each architecture was analyzed to understand its design approach and its contribution toward improving the performance of the FFT processor.

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The selected reversible FFT architectures were then compared using important VLSI and reversible computing performance metrics, including quantum cost, garbage outputs, constant inputs, gate count, propagation delay, power consumption, silicon area, hardware complexity, and Power-Delay Product (PDP). The review also examines the impact of different reversible gates and adder designs on the efficiency of butterfly operations, which represent the computational core of the Radix-2 FFT algorithm. Comparative analysis tables were prepared to summarize the advantages, limitations, and implementation characteristics of each reported design.

Finally, the reviewed literature was critically analyzed to identify current research trends, existing limitations, and open research challenges in reversible FFT implementation. Based on the comparative study, potential future research directions are proposed, including the development of quantum-aware reversible FFT architectures, optimized reversible arithmetic units, pipelined and parallel reversible butterfly processors, and scalable implementations for quantum computing, nanotechnology, digital signal processing, artificial intelligence, and low-power VLSI systems. This methodology provides a comprehensive framework for evaluating existing reversible Radix-2 FFT architectures and identifying efficient design strategies for next-generation energy-efficient signal processing hardware.

Reversible Gate:

A reversible gate is a fundamental building block of reversible logic circuits in which there exists a one-to-one correspondence between the input and output vectors. Unlike conventional logic gates, reversible gates do not lose information during computation, enabling the original inputs to be uniquely reconstructed from the outputs. According to Landauer's principle, the loss of one bit of information in an irreversible circuit dissipates a minimum energy of , where is the Boltzmann constant and is the absolute temperature. Reversible logic eliminates this information loss, making it highly suitable for low-power VLSI systems, quantum computing, nanotechnology, optical computing, and digital signal processing (DSP).

In a reversible circuit, the number of inputs is always equal to the number of outputs, and fan-out and feedback are generally avoided to preserve reversibility. The efficiency of a reversible gate is evaluated using several design metrics, including quantum cost, garbage outputs, constant inputs, gate count, propagation delay, and hardware complexity. Lower values of these parameters indicate a more efficient reversible circuit. Because FFT processors require numerous arithmetic operations, reversible gates play a crucial role in designing energy-efficient butterfly units and arithmetic circuits.

IV. CONCLUSION

This review presented a comprehensive analysis of Reversible Radix-2 Fast Fourier Transform (FFT) architectures implemented using various reversible logic gates and reversible adder designs. The study examined widely used reversible gates, including the Feynman Gate, Toffoli Gate, Fredkin Gate, Peres Gate, HNG Gate, TSG Gate, and BKG

Gate, along with different reversible adder architectures such as Ripple Carry Adder (RCA), Carry Look-Ahead Adder (CLA), Carry Save Adder (CSA), Carry Select Adder (CSLA), and Modified Carry Select Adder (MCSLA). The reviewed literature demonstrates that reversible logic significantly reduces information loss and energy dissipation while improving computational efficiency, making it a promising technology for low-power VLSI and quantum computing applications.

The comparative analysis indicates that the performance of a reversible Radix-2 FFT processor largely depends on the selection of reversible gates and arithmetic units employed in the butterfly structure. Optimized reversible adder architectures offer lower quantum cost, garbage outputs, constant inputs, propagation delay, hardware complexity, and power consumption, thereby enhancing the overall efficiency of FFT implementations. Although considerable progress has been achieved in reversible FFT design, challenges such as minimizing quantum cost, reducing garbage outputs, improving scalability, and simplifying circuit complexity remain active research areas.

Overall, reversible logic provides an effective solution for developing high-speed, low-power, and energy-efficient FFT processors suitable for digital signal processing, wireless communication, image processing, biomedical engineering, nanotechnology, and quantum computing. Future research should focus on designing optimized reversible butterfly units, integrating advanced reversible adder architectures, developing pipelined and parallel reversible FFT processors, and exploring quantum-aware synthesis techniques to further improve performance. These advancements will contribute to the realization of next-generation energy-efficient VLSI systems and scalable quantum computing architectures.

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